PLL NOISE SMOOTHING USING DUAL-MODULUS INTERLEAVING

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to phase locked loops (PLLs).

2. State of the Art

Practically all modern signal generators and radio communications equipment make widespread use of PLLs. A known PLL is shown in Figure 1. A reference frequency f_{in} is applied to a phase or phase/frequency detector, to which is also applied a feedback signal derived from an output frequency signal f_{out} of the PLL. The detector produces an error signal, which is filtered by a loop filter. An output signal of the loop filter is applied to a voltage-controlled oscillator (VCO), which produces the output frequency signal f_{out}. Commonly, a programmable divide-by-N counter divides down the output frequency signal f_{out} to produce a lower frequency signal that is then applied to the detector. In this manner, an output frequency signal can be generated that is some multiple of the reference frequency. Such divide-by-N counters are typically realized in CMOS.

At very high frequencies (such as those used in cellular radiotelephones), however, the speed capability of even the fastest CMOS circuit is quickly exceeded. In this instance, a dual-modulus prescaler is commonly used in which the difference between one divide modulus (P) and the other divide modulus (P + 1) is one. In such an arrangement, shown in Figure 2, a high-speed (e.g., ECL) dual-modulus counter is followed by a lower-speed (e.g., CMOS) programmable counter. The lower-speed counter controls which modulus of the dual-modulus prescaler is active at a given time via a modulus control signal MC. The use of multiple moduli enables a full range of effective divisors to be obtained.

One construction of such a circuit is shown in Figure 3, in which the dual-modulus counter is followed by a pair of lower-speed (e.g., CMOS) programmable counters. In the circuit of Figure 3, the reference and output frequencies are related

as follows:

$$\begin{aligned} f_{out} &= N \cdot f_{in} \\ &= (QP + R)f_{in} \\ &= ((Q - R)P + R(P + 1))f_{in} \end{aligned}$$

where Q is the quotient of the integer division N/P and R is the remainder of the integer division N/P. The value Q is used to preset a "tens" counter (so-called because its effect is multiplied by the modulus P) and R is used to preset a "ones" counter (the effect of which is not multiplied by the modulus). The value Q must be greater than or equal to the value R. With this restriction, the minimum division ratio achievable to guarantee continuous coverage of the possible integer divisors N using such a circuit is, in general, P(P - 1).

Assume, for example, that a 10/11 dual-modulus prescaler (P = 10) is used and that a desired output frequency is 197 times the reference frequency. Using the foregoing formula, Q might be 19 and R might be 7. (Note that R < P always.) These values are preset into the respective counters. With a non-zero value loaded into the R counter, the dual-modulus prescaler is set to divide by P + 1 at the start of the cycle. (The period of the cycle is given by the reciprocal of the reference frequency.) The output from the dual-modulus prescaler clocks both counters. When the R counter reaches zero, it ceases counting and sets the dual-modulus prescaler to divide by P. Only the Q counter is then clocked. Such a cycle is illustrated in Figure 4. When the Q counter reaches zero, the initial values are again loaded into the counters and the next cycle begins.

In such a circuit, the modulus control signal for controlling the dual-modulus prescaler can generate considerable noise within the frequency band of the reference signal, since the period of this modulus control signal is equal to the period of the PLL reference signal. Various filtering strategies have been used to attack

this problem. An effective, low-cost solution to this problem remains a long-standing need.

SUMMARY OF THE INVENTION

The present invention, generally speaking, achieves noise spreading within a PLL using a dual-modulus prescaler by interleaving the division moduli. Within a given cycle, "ones" and "tens" are not all counted consecutively. Instead, ones and tens are interleaved. In one embodiment of the invention, the R count is doubled and the output of the R counter is toggled between high and low states. (The Q counter may remain unmodified.) In another embodiment of the invention, ones and tens are interleaved in accordance with a ratio q:r. By so interleaving the modulus, the effect is to spread the noise resulting from the output signal of the dual-modulus prescaler over a wider frequency range. The prescaler noise level is greatly reduced, particularly within the frequency band of the reference frequency.

BRIEF DESCRIPTION OF THE DRAWING

The present invention may be further understood from the following description in conjunction with the appended drawing. In the drawing:

Figure 1 is a block diagram of a conventional PLL using a divide-by-N counter;

Figure 2 is a block diagram of a conventional PLL using a dual-modulus prescaler;

Figure 3 is a more detailed block diagram of one realization of the circuit of Figure 2;

Figure 4 is a timing diagram illustrating operation of the PLL of Figure 2;

Figure 5 is a diagram illustrating the principle of the invention in accordance with one embodiment thereof;

Figure 6 is a block diagram of a PLL in accordance with one aspect of the present invention;

Figure 7 is a timing diagram illustrating operation of the PLL of Figure 6;

Figure 8 is a waveform display showing noise levels using a conventional

PLL circuit; and

Figure 9 is a waveform display showing noise levels using the present PLL circuit.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The modulus interleaving technique of the present invention may be applied in various forms with varying degrees of sophistication and complexity. A simple but effective implementation of modulus interleaving is illustrated in Figure 5. In this implementation, the Q count and the Q counter are left unchanged. The R count is doubled, and the R counter is toggled. For example, if the R count would normally be 15 with the counter output being held low for 15 counts, instead the count is doubled to 30. The counter output, instead of being held low continuously, is toggled, i.e., low for 1 count, high for 1 count, low for 1 count, etc. The overall effect is the same as in the conventional case--referring again to the foregoing equations, the effect is to replace R with 2R/2. The difference is that the energy spectrum of the modulus control signal is shifted above and away from the PLL reference frequency. If desired, the same measure may be taken with respect to Q. In general, R (and Q, if desired) may be replaced by mR/m, where m is the number of moduli of the prescaler. For a dual modulus prescaler, m = 2.

In other arrangements, it may be advantageous to be able to control the distribution of pulses within the modulus control signal. Referring now to Figure 6, a block diagram is shown of a PLL circuit in accordance with another embodiment of the present invention. As compared to the PLL circuit of Figure 2, the R counter and the Q counter are modified by the addition of an r counter and an q counter, respectively. The resulting R counter counts R total counts, r at a time. The resulting Q counter counts Q total counts, q at a time. In accordance with an exemplary embodiment, the apparatus operates in the following manner.

As in the prior art circuit, with a non-zero value loaded into the R counter, the dual-modulus prescaler is set to divide by P + 1 at the start of the cycle. The

output from the dual-modulus prescaler clocks both counters. When the r counter reaches zero, the R counter ceases counting and sets the dual-modulus prescaler to divide by P. Only the Q counter is then clocked. When the q counter reaches zero, the initial values r and q are again loaded into the counters and the next subcycle begins. During the final subcycle, the R counter counts down to zero, after which the Q counter counts down to zero. Such operation is illustrated in Figure 7, with (R, r) = (7, 1) and (Q, q) = (8 , 1). Note that r and q need not be one; the only requirements are that $R \leq Q$, $r \leq R$, and $q \leq Q$. (The case r = R and q = Q represents the conventional operating method.)

The noise spreading effect of the present modulus interleaving technique may be observed by comparing Figure 8 and Figure 9. Figure 8 is a plot of the energy within the signal present on the modulus control line in accordance with the traditional modulus control setup of Figures 3 and 4. Excluding zero hertz, the noise margin at the first noise peak is about -5dbm. Figure 9 is a plot of the energy within the signal present on the modulus control line in accordance with the present modulus control setup of Figures 6 and 7. Excluding zero hertz, the noise margin at the first noise peak is about -25dbm. Thus, this example demonstrates a reduction in the noise from the modulus control signal at the reference frequency of 20dB. Note that there are no additional components or extra filtering required by this method. There is essentially no increase in the cost of a PLL incorporating the present invention. Note further that this interleaving is readily expanded to higher order multi-modulus prescaling, such as 3-modulus and 4-modulus prescalers.

It will be appreciated by those of ordinary skill in the art that the invention can be embodied in other specific forms without departing from the spirit or essential character thereof. The presently disclosed embodiments are therefore considered in all respects to be illustrative and not restrictive. The scope of the invention is indicated by the appended claims rather than the foregoing description, and all changes which come within the meaning and range of equivalents thereof are intended to be embraced therein.